IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (previously presented) A method for designing a semiconductor having a computer for inserting a dummy pattern between design patterns, the method comprising the steps of:

dividing a layout pattern for a layout layer in a semiconductor device into divided areas;

inserting a dummy pattern between design patterns in the divided areas;

calculating the density of the dummy pattern and the design patterns in each of the divided areas; and

changing pattern rules for the dummy pattern so that the density will be desired values.

2. (previously presented) The method for designing a semiconductor device according to claim 1, wherein the design patterns are wiring patterns and the layout layer is a wiring layer.

3. (previously presented) The method for designing a semiconductor device according to claim 1, wherein:

division specification information regarding size of the divided areas is accepted; and

the layout pattern is divided into divided areas having the size of which is specified by the division specification information.

4. (previously presented) The method for designing a semiconductor device according to claim 1, wherein:

generated dummy specification information regarding the specification of the divided area in which the dummy pattern is to be inserted is accepted; and

the dummy pattern is inserted between design patterns in the divided area specified by the generated dummy specification information.

5. (previously presented) The method for designing a semiconductor device

according to claim 1, wherein:

dummy rule information regarding pattern rules for the dummy pattern inserted between the design patterns is accepted; and

the dummy pattern having the pattern rules for which are based on the dummy rule information is inserted between the design patterns.

6. (previously presented) The method for designing a semiconductor device according to claim 1, wherein the dummy pattern is inserted between design patterns in an area including the divided area and a divided area adjacent to the divided area.

7. (previously presented) The method for designing a semiconductor device according to claim 1, wherein if the density does not match the desired values, the density of the dummy pattern and the design patterns in an area obtained by enlarging the divided area where the density was calculated is calculated.

8. (previously presented) The method for designing a semiconductor device according to claim 1, wherein if the density does not match the desired values, the density of the dummy pattern and the design patterns in an area including the divided area where the density was calculated and a divided area adjacent to the divided area is calculated.

9. (previously presented) The method for designing a semiconductor device according to claim 1, wherein the density of design patterns and dummy patterns on the entire layout pattern is calculated.

10. (previously presented) A program for designing a semiconductor device which inserts a dummy pattern between design patterns, the program making a computer perform the processes of:

dividing a layout pattern for a layout layer in a semiconductor device into divided areas;

inserting a dummy pattern between design patterns in the divided areas;

calculating the density of the dummy pattern and the design patterns in each of the divided areas; and

changing pattern rules for the dummy pattern so that the density will be desired values.

11. (previously presented) A computer-readable record medium which stores a

program for designing a semiconductor device which inserts a dummy pattern between design patterns, the program making a computer perform the processes of:

dividing a layout pattern for a layout layer in a semiconductor device into divided areas;

inserting a dummy pattern between design patterns in the divided areas;

calculating the density of the dummy pattern and the design patterns in each of the divided areas; and

changing pattern rules for the dummy pattern so that the density will be desired values.

12. (previously presented) An apparatus for designing a semiconductor device which inserts a dummy pattern between design patterns, the apparatus comprising:

a dividing section for dividing a layout pattern for a layout layer in a semiconductor device into divided areas;

an inserting section for inserting a dummy pattern between design patterns in the divided areas;

a calculating section for calculating the density of the dummy pattern and the design patterns in each of the divided areas; and

a changing section for changing pattern rules for the dummy pattern so that the density will be desired values.